TSIA 2022 半導體獎

獎項介紹

「TSIA 半導體獎」是台灣半導體產業協會於 2014 年起，為了獎勵國內積極從事半導體之學術研究、發明或致力投入產業合作並有具體貢獻者而設立。

此獎項之得獎人由本會遴選委員會評選，遴選委員由在半導體領域已有卓越成就之學者、專家及產業領導者擔任。

今年具博士學位之新進研究人員半導體獎由中山大學奈米科技研發中心陳柏勳助理教授獲獎；博士研究生半導體獎得獎者，分別由台大、陽明交通、成大、清大、中山等 5 校 11 位博士班同學獲獎，本會期許得獎人以成為台灣半導體產業優秀貢獻者為目標，再接再厲，為台灣半導體產業之永續發展而戮力前進。

贊助單位：理監事公司

力成科技股份有限公司	力晶科技股份有限公司	力晶積成電子製造股份有限公司
工業技術研究院	日月光半導體製造股份有限公司	世界先進積體電路股份有限公司
立錡科技股份有限公司	台灣積體電路製造股份有限公司	欣銓科技股份有限公司
矽品精密工業股份有限公司	南亞科技股份有限公司	凌陽科技股份有限公司
創意電子股份有限公司	華邦電子股份有限公司	鈺創科技股份有限公司
漢民科技股份有限公司	聯發科技股份有限公司	聯華電子股份有限公司

◎ 以上依公司筆劃順序排列

陳柏勳 Po-Hsun Chen

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具博士學位之新進研究人員

獲獎摘要

陳柏勳博士於 2018 年取得國立中山大學物理博士學位，博士班期間即致力於電子元件可靠度研究與奈米半導體材料應用，研究主題包括新穎非揮發電阻式記憶體、銦鎵鋅氧薄膜電晶體與氧化釩選擇器等多種電子元件。目前陳博士亦致力於低溫超高壓退火 (Super-high Pressure Annealing, SPA) 與超臨界流體 (Super Critical Fluid, SCF) 製程技術，並運用於電子元件與材料，藉以修補缺陷並提升元件性能與材料特性。

得獎經歷

- 2021 台灣電子材料與元件協會『傑出青年獎』
- 2021 潘文淵文教基金會『考察研究獎助金』
- 2018 臺灣綜合大學系統『年輕學者創新成果選拔佳作獎』
- 2018 國立中山大學『優秀博士研究生畢業論文獎』
- 2017 台灣半導體產業協會『半導體獎：博士研究生』
- 2017 IEEE Electron Devices Society PhD Student Fellowship Award

重要學術著作

1. **Po-Hsun Chen,** Chih-Yang Lin, Ting-Chang Chang, Jason K. Eshraghian, Yu-Ting Chao, Wei D. Lu, Simon M. Sze (2022, Jan). Investigating Selectorless Property within Niobium Devices for Storage Applications. ACS Applied Materials & Interfaces, 14(1), 2343-2350.
2. **Po-Hsun Chen,** Chen-Yi Hsieh, Yu-Ting Su (2021, Jul). Investigation of Abnormal Forming Process Current Caused by Copper Diffusion in Cu/GeSO/TiN Resistance Random Access Memory. Materials Chemistry and Physics, 267, pp 124654.
3. **Po-Hsun Chen,** Chih-Yang Lin, Jing-Shuen Chang, Yi-Ting Tseng, Jen-Wei Huang (2021, Apr). Enhanced switching performance of resistance random access memories by an inserted copper tellurium layer. Journal of Physics D: Applied Physics, 54(16), 165110.
4. Chih-Yang Lin, Jia Chen, **Po-Hsun Chen,** Ting-Chang Chang, Yuting Wu, Jason K. Eshraghian, John Moon, Sangmin Yoo, Yu-Hsun Wang, Wen-Chung Chen, Zhi-Yang Wang, Hui-Chun Huang, Yi Li, Xiangshui Miao, Wei D. Lu, Simon M. Sze (2020, Oct). Adaptive Synaptic Memory via Lithium Ion Modulation in RRAM Devices. SMALL, 16(42), 2003964.
5. Ting-Chang Chang, **Po-Hsun Chen,** Chih-Yang Lin, Chih-Cheng Shih (2020, Aug). Low Temperature Defect Passivation Technology for Semiconductor Electronic Devices - Supercritical Fluids Treatment Process. Materials Today Physics, 14, 100225.
6. Chih-Yang Lin, **Po-Hsun Chen,** Ting-Chang Chang, Wei-Chen Huang, Yong-Fang Tan, Yun-Hsuan Lin, Wen-Chung Chen, Chun-Chu Lin, Yao-Feng Chang, Ying-Chen Chen, Hui-Chun Huang, Xiao-Hua Ma, Yue Hao, Simon M Sze (2020, Jun). A Comprehensive Study of Enhanced Characteristics with Localized Transition in Interface-type Vanadium-based Devices. Materials Today Physics, 13, pp. 100201.
7. **Po-Hsun Chen,** Chen-Yi Hsieh, Hong-Yi Yang (2020, Jun). Effects of Charge Quantity Induced by Different Forming Methods in Solid Electrolyte GeSO-based Resistance Switching Device with Copper Electrode. IEEE Transactions on Electron Devices, 67(6), 2324-2328.
8. **Po-Hsun Chen,** Hao-Xuan Zheng, Yu-Ting Su (2020, May). Incorporation of a bipolar incremental step pulse programming with thermal forming to reduce the forming voltage in 1T1R structure resistance random access memory. Applied Physics Express, 13(5), 056503.
9. **Po-Hsun Chen,** Hong-Yi Yang, Yu-Ting Su, Chia-Min Tsou (2020, Feb). Fully Transparent Resistance Switching Memristor Based on Indium-Tin-Oxide Material. Journal of Micromechanics and Microengineering, 30(4), 045003.
10. **Po-Hsun Chen,** Yu-Ching Tsao, Yu-Chieh Chien, Hsiao-Cheng Chiang, Hua-Mao Chen, Ying-Hsin Lu, Chih-Cheng Shih, Mao-Chou Tai, Guan-Fu Chen, Yu-Lin Tsai, Hui-Chun Huang, Tsung-Ming Tsai, Ting-Chang Chang (2019, Aug). A Dual-Gate InGaZnO4-Based Thin-Film Transistor for High-Sensitivity UV Detection. Advanced Materials Technologies, 4(8), 1900106.

指導教授　張鼎張 教授

現職　・國立中山大學物理學系 / 講座教授
學歷　・國立陽明交通大學 / 電子工程學系博士
經歷　・國立中山大學 / 物理學系教授
・ IEEE Fellow
・國家奈米實驗室研究員

推薦專家　施敏 院士

現職　・國立陽明交通大學 / 電子研究所終身講座教授
學歷　・美國史丹佛大學 / 電機工程博士
經歷　・國家實驗研究院榮譽顧問
・ IEEE Life Fellow
・中央研究院院士
・美國國家工程院院士
・教育部國家講座教授

杜建德 Chien-Te Tu

博士研究生

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獲獎摘要

杜建德同學於國立臺灣大學電子工程學研究所攻讀博士班，研究領域為高效能鍺矽與鍺錫 3D 場效電晶體之製程整合與元件特性分析。開發垂直堆疊閘極環繞式電晶體 (stacked GAAFETs) 以及新穎結構樹狀通道電晶體 (TreeFET) 之製程與優化。相關研究成果發表於 IEEE 頂尖國際會議 IEDM 與 Symposium on VLSI Technology 和一流之 IEEE EDL 與 TED 國際期刊，有 5 項美國專利申請中。成果豐碩，難能可貴。

得獎經歷 / 專利

- 2020 台積電博士班獎學金
- 2019 年臺大電子所學生傑出研究獎
- 以第一發明人申請 3 篇美國專利，以共同發明人申請 2 篇美國專利
- 以第七發明人發表美國專利，Patent number：USP 11,233,120
- 2019 - 2021 台積電 - 臺大聯合研發中心獎助學金

重要學術著作

1. **Chien-Te Tu,** Yu-Shiang Huang, Fang-Liang Lu, Hsiao-Hsuan Liu, Chung-Yi Lin, Yi-Chun Liu, and C. W. Liu, "First Vertically Stacked Tensily Strained $Ge_{0.98}Si_{0.02}$ nGAAFETs with No Parasitic Channel and L_G = 40 nm Featuring Record I_{ON} = 48 μA at V_{OV}=V_{DS}= 0.5V and Record $G_{m,max}$(μS/ μm) / SS_{SAT}(mV/dec)= 8.3 at V_{DS}=0.5V," pp. 681-684, International Electron Devices Meeting (IEDM), 2019.
2. **Chien-Te Tu,** Wan-Hsuan Hsieh, Bo-Wei Huang, Yu-Rui Chen, Yi-Chun Liu, Chung-En Tsai, Shee-Jier Chueh, and C. W. Liu, "Experimental Demonstration of TreeFETs Combining Stacked Nanosheets and Low Doping Interbridges by Epitaxy and Wet Etching," IEEE Electron Device Letters, Vol. 43, No. 5, pp. 682-685, May 2022.
3. **Chien-Te Tu,** Yu-Shiang Huang, Chun-Yi Cheng, Chung-En Tsai, Jyun-Yan Chen, Hung-Yu Ye, Fang-Liang Lu, and C. W. Liu, "Uniform 4-Stacked $Ge_{0.9}Sn_{0.1}$ Nanosheets Using Double $Ge_{0.95}Sn_{0.05}$ Caps by Highly Selective Isotropic Dry Etch," IEEE Transactions on Electron Devices, Vol. 68, No. 4, pp. 2071-2076, Apr. 2021.
4. (invited) **Chien-Te Tu,** Bo-Wei Huang, Chung-En Tsai, Yi-Chun Liu, and C. W. Liu, "GeSn/GeSi Stacked Channel Transistors," International Conference on Solid State Devices and Materials (SSDM), Sept. 2021.
5. Chung-En Tsai, Yi-Chun Liu, **Chien-Te Tu,** Bo-Wei Huang, Sun-Rong Jan, Yu-Rui Chen, Jyun-Yan Chen, Shee-Jier Chueh, Chun-Yi Cheng, Chia-Jung Tsen, Yichen Ma, and C. W. Liu, "Highly Stacked 8 $Ge_{0.9}Sn_{0.1}$ Nanosheet pFETs with Ultrathin Bodies (~3nm) and Thick Bodies (~30nm) Featuring the Respective Record I_{ON}/I_{OFF} of 1.4E7 and Record I_{ON} of 92 μA at V_{OV}=V_{DS}= -0.5V by CVD Epitaxy and Dry Etching," pp. 569-572, International Electron Devices Meeting (IEDM), 2021.
6. Yi-Chun Liu, **Chien-Te Tu,** Chung-En Tsai, Yu-Rui Chen, Jyun-Yan Chen, Sun-Rong Jan, Bo-Wei Huang, Shee-Jier Chueh, Chia-Jung Tsen, and C. W. Liu, "First Highly Stacked $Ge_{0.95}Si_{0.05}$ nGAAFETs with Record I_{ON} = 110 μA (4100 μA/ μm) at V_{OV}=V_{DS}=0.5V and High $G_{m,max}$ = 340 μS (13000 μS/ μm) at V_{DS}=0.5V by Wet Etching," Symposia on VLSI Technology and Circuits (VLSI), 2021.
7. Chung-En Tsai, Yu-Rui Chen, **Chien-Te Tu,** Yi-Chun Liu, Jyun-Yan Chen, and C. W. Liu, "First Demonstration of Multi-VT Stacked $Ge_{0.87}Sn_{0.13}$ Nanosheets by Dipole-Controlled ALD WNxCy Work Function Metal with Low Resistivity and Thermal Budget ≤ 400°C," Symposia on VLSI Technology and Circuits (VLSI), 2021.
8. Yu-Shiang Huang, Chung-En Tsai, **Chien-Te Tu,** Jyun-Yan Chen, Hung-Yu Ye, Fang-Liang Lu, and C. W. Liu, "First Demonstration of Uniform 4-Stacked $Ge_{0.9}Sn_{0.1}$ Nanosheets with Record I_{ON}=73 μA at V_{OV}=V_{DS}= -0.5V and Low Noise Using Double $Ge_{0.95}Sn_{0.05}$ Caps, Dry Etch, Low Channel Doping, and High S/D Doping," pp. 23-26, International Electron Devices Meeting (IEDM), 2020.
9. Yu-Shiang Huang, Fang-Liang Lu, **Chien-Te Tu,** Jyun-Yan Chen, Chung-En Tsai, Hung-Yu Ye, Yi-Chun Liu and C. W. Liu, "First Demonstration of 4-Stacked $Ge_{0.915}Sn_{0.085}$ Wide Nanosheets by Highly Selective Isotropic Dry Etching with High S/D Doping and Undoped Channels," Symposia on VLSI Technology and Circuits (VLSI), 2020.
10. Yu-Shiang Huang, Chung-En Tsai, **Chien-Te Tu,** Hung-Yu Ye, Yi-Chun Liu, Fang-Liang Lu, and C. W. Liu, "First Stacked $Ge_{0.88}Sn_{0.12}$ pGAAFETs with Cap, L_G=40nm, Compressive Strain of 3.3%, and High S/D Doping by CVD Epitaxy Featuring Record I_{ON} of 58 μA at V_{OV}=V_{DS}= -0.5V, Record $G_{m,max}$ of 172 μS at V_{DS}= -0.5V, and Low Noise," pp. 689-692, International Electron Devices Meeting (IEDM), 2019.

指導教授　劉致為 教授

現職 ・ Distinguished / Chair Professor, National Taiwan University

學歷 ・ Ph.D. 1994 Electrical Engineering, Princeton University
・ M.S. 1987 and B.S. 1985, National Taiwan University

經歷 ・ IEEE Fellow (2018~)
・ Deputy General Director (副主任 , 2008~2013) / Senior full researcher (資深研究員 , 2011~), National Nano Device Labs
・ Research Director / Senior full researcher (資深研究員), ERSO / ITRI (2002 ~ 2005)

廖唯邦 Wei-Bang Liao

博士研究生

國立臺灣大學 材料科學與工程學系

獲獎摘要

廖唯邦同學自2020年起於國立臺灣大學材料科學與工程學系研究所攻讀博士班。研究領域為自旋霍爾效應 (Spin Hall effect)，和自旋軌道矩式磁阻記憶體 (Spin-orbit Torque Magnetic Random Assess Memory, SOT-MREM)。曾參與 The Magnetism and Magnetic Materials Conference (MMM)、IEEE Intermag、American Physical Society (APS) 等國際會議，並於會議中發表相關研究成果。

得獎經歷

- 2020 台積電博士生獎學金
- 2020 科技部優秀博士生獎學金
- 2019 台灣磁性年會海報優等獎

重要學術著作

1. C.-W. Peng†, **W.-B. Liao†,** T.-Y. Chen, and C.-F. Pai, "Efficient Spin-Orbit Torque Generation in Semiconducting WTe_2 with Hopping Transport", ACS Appl. Mater. Interfaces 13, 15950 (2021).
2. **W.-B. Liao,** T.-Y. Chen, Y.-C. Hsiao, and C.-F. Pai, "Pulse-width and Temperature Dependence of Memristive Spin-Orbit Torque Switching", Applied Physics Letter 117, 182402 (2020).
3. **W.-B. Liao,** T.-Y. Chen, Y. Ferrante, S. S. P. Parkin, and C.-F. Pai, "Current-induced magnetization switching by the high spin Hall conductivity α-W," Physica Status Solidi (RRL) – Rapid Research Letters 13, 1900408 (2019).
4. N. Murray, **W.-B. Liao,** T.-C. Wang, L.-J. Chang, L.-Z. Tsai, T.-Y. Tsai, S.-F. Lee, and C.-F. Pai, "Field-free spin-orbit torque switching through domain wall motion," Physical Review B 100, 104441 (2019).
5. T.-Y. Chen, **W.-B. Liao,** T.-Y. Chen, T.-Y. Tsai, C.-W. Peng, and C.-F. Pai, "Current-induced spin-orbit torque efficiencies in W/Pt/Co/Pt heterostructures," Applied Physical Letters 116, 072405 (2020).
6. T.-Y. Chen, H.-I. Chan, **W.-B. Liao,** and C.-F. Pai, "Current-induced spin-orbit torque and field-free switching from Mo-based magnetic heterostructures," Physical Review Applied 10, 044038 (2018).
7. T.-Y. Chen, C.-W. Peng, T.-Y. Tsai, **W.-B. Liao,** C.-T. Wu, H.-W. Yen, and C.-F. Pai*, "Efficient Spin-Orbit Torque Switching with Nonepitaxial Chalcogenide Heterostructures," ACS Appl. Mater. Interfaces 12, 7788 (2020).

指導教授　白奇峰 副教授

現職　・國立臺灣大學

學歷　・Ph.D. in Applied and Engineering Physics, Cornell University
・B.Eng. in MSE and B.Sc. in Physics, National Taiwan University

經歷　・Vice Chair, IEEE Magnetic Society, Taiwan Chapter (2019 - present)
・Consulting Research Fellow, MRAM Team, ITRI (2016 - 2022)
・Post-doctoral Research Associate, DMSE, MIT (2014 - 2016)

鄧傑方 Chieh-Fang Teng

博士研究生

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獲獎摘要

鄧傑方同學自 2017 年起大學逕讀國立臺灣大學電子工程學研究所博士班，研究領域為應用深度學習技術輔助 5G 通訊極化碼解碼器 (Polar Decoder) 性能，包含提升置信傳播 (Belief Propagation) 解碼演算法收斂速度，並提出相對應硬體實現架構。相關研究成果發表於 IEEE 頂尖國際會議 Symposium on VLSI Circuits 和頂尖國際期刊 IEEE TCAS-I、TSP。在學期間成果豐碩並獲多項獎項肯定，難能可貴。

得獎經歷

- 2021 科技部千里馬計畫
- 2021 中技社研究獎學金
- 2020 旺宏金矽獎 - 評審團鑽石大賞、最佳創意獎
- 2020 臺大傑出表現獎
- 2020 臺大電子所學生傑出研究獎
- 2020 臺大 1975 級電機系系友科技研究創新獎 - 特別獎
- 2017 - 2021 聯發科技創新研究中心獎學金

重要學術著作

1. S.-S. Wong, **C.-F. Teng,** and A.-Y. A. Wu, “Two-Step Codebook-Assisted Alternating Minimization (CA-AltMin) for Low-Complexity Hybrid Beamforming Design,” IEEE Communications Letters, 2021.
2. **C.-F. Teng** and A.-Y. A. Wu, “A 7.8-13.6 pJ/b Ultra-Low Latency and Reconfigurable Neural Network-Assisted Polar Decoder with Multi-Code Length Support,” IEEE Transactions on Circuits and Systems I (TCAS-I), 2021.
3. **C.-F. Teng** and A.-Y. A. Wu, “Convolutional Neural Network-Aided Tree-Based Bit-Flipping Framework for Polar Decoder Using Imitation Learning,” IEEE Transactions on Signal Processing (TSP), 2021.
4. **C.-F. Teng,** C.-Y. Chou, C.-H. Chen, and A.-Y. A. Wu, “Accumulated Polar Feature-based Deep Learning for Efficient and Lightweight Automatic Modulation Classification with Channel Compensation Mechanism,” IEEE Transactions on Vehicular Technology (TVT), 2020.
5. **C.-F. Teng** and Y.-L. Chen, “Syndrome-Enabled Unsupervised Learning for Neural Network-Based Polar Decoder and Jointly Optimized Blind Equalizer,” IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), 2020.
6. Y.-S. Tai, **C.-F. Teng,** C.-Y. Chang, and A.-Y. A. Wu, “Compression-aware Projection with Greedy Dimension Reduction for Convolutional Neural Network Activations,” IEEE Int. Conf. Acoust., Speech, Signal Process. (ICASSP), 2022.
7. **C.-F. Teng,** A. K.-S. Ho, C.-H. D. Wu, S.-S. Wong, and A.-Y. A. Wu, “Convolutional Neural Network-aided Bit-flipping for Belief Propagation Decoding of Polar Codes,” IEEE Int. Conf. Acoust., Speech, Signal Process. (ICASSP), 2021.
8. **C.-F. Teng,** C.-H. Chen, and A.-Y. A. Wu, “An Ultra-Low Latency 7.8-13.6 pJ/b Reconfigurable Neural Network-Assisted Polar Decoder with Multi-Code Length Support,” IEEE Symposia on VLSI Technology and Circuits, 2020.
9. C.-H. Chen, **C.-F. Teng,** and A.-Y. A. Wu, “Low-Complexity LSTM-Assisted Bit-Flipping Algorithm for Successive Cancellation List Polar Decoder,” IEEE Int. Conf. Acoust., Speech, Signal Process. (ICASSP), 2020.
10. **C.-F. Teng,** C.-H. D. Wu, A. K.-S. Ho, and A.-Y. A. Wu, “Low-complexity Recurrent Neural Network-based Polar Decoder with Weight Quantization Mechanism,” IEEE Int. Conf. Acoust., Speech, Signal Process. (ICASSP), 2019.

指導教授　吳安宇 教授

現職
- 國立臺灣大學 電機系 / 電子所特聘教授

學歷
- Ph.D. in Electrical Engineering, University of Maryland, 1995
- M.S. in Electrical Engineering, University of Maryland, 1992
- B.S. in Electrical Engineering, National Taiwan University, 1987

經歷
- (IEEE 期刊總主編) Editor-in-Chief (EiC), IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS) (2020~2021)
- 臺灣大學電子所所長 (2016~2019)
- IEEE Fellow (2015~)
- 工研院系統晶片中心副主任 (2007~2009)
- Member of Technical Staff, AT&T Bell Labs./Microelectronics (1995~1996)

謝伊妍 Yi-Yen Hsieh

博士研究生

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獲獎摘要

謝伊妍同學於國立臺灣大學電子工程學研究所攻讀博士班，研究領域為具備人工智慧之數位高效節能硬體加速器設計，並應用於生醫訊號處理與機器學習等相關領域。其針對影像轉換的生成對抗式網路晶片設計研究成果，發表於 2020 IEEE ISCAS，並獲得 2021 VLSI-CAD 最佳論文獎。其針對癲癇預測開發之神經訊號處理器，為世界上第一顆可支持癲癇預測之極低功耗整合晶片設計，相關研究成果發表於 2022 IEEE 國際頂尖固態電路會議 ISSCC，並獲選為大會重點論文，同時得到當年度 IEEE SSCS STGA 獎項。

得獎經歷

- 2022 IEEE Solid-State Circuits Society Student Travel Grant Award (STGA)
- 2021 臺大 1975 級電機系系友科技研究創新獎
- 2021 VLSI-CAD 會議大會最佳論文獎
- 2018 臺大電子所產業贊助獎學金：意騰科技
- 2017 臺大電子所產業贊助獎學金：矽創電子

重要學術著作

1. **Y.-Y. Hsieh,** Y.-C. Lin, and C.-H. Yang, "A 96.2nJ/class neural signal processor with adaptable intelligence for seizure prediction," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2022.
2. **Y.-Y. Hsieh,** Y.-C. Lee, and C.-H. Yang, "An energy-efficient CycleGAN accelerator for edge AI devices," VLSI-CAD, Aug. 2021.
3. S.-A. Huang, **Y.-Y. Hsieh,** and C.-H. Yang, "Design optimization for ADMM-based SVM training processor for edge computing," International Conference on Artificial Intelligence Circuits and Systems (AICAS), May 2021.
4. **Y.-Y. Hsieh,** Y.-C. Lee, and C.-H. Yang, "A CycleGAN accelerator for unsupervised learning on mobile devices," IEEE International Symposium on Circuits and Systems (ISCAS), Oct. 2020.
5. C. Yu, R. E. Zezario, S.-S. Wang, J. Sherman, **Y.-Y. Hsieh,** X. Lu, H.-M. Wang, and Y. Tsao, "Speech enhancement based on denoising autoencoder with multi-branched encoders," IEEE/ACM Transactions on Audio, Speech, and Language Processing (TASLP), vol. 28, pp.2756-2769, Oct. 2020.
6. H.-T. Chiang, **Y.-Y. Hsieh,** S.-W. Fu, K.-H. Hung, Y. Tsao, and S.-Y. Chien, "Noise reduction in ECG signals using fully convolutional denoising autoencoders," IEEE Access, vol. 7, pp. 60806-60813, Apr. 2019.
7. K.-Y. Yeh, T.-H. Lin, **Y.-Y. Hsieh,** C.-M. Chang, Y.-J. Yang, and S.-S. Lu, "A cuffless wearable system for real-time cutaneous pressure monitoring with cloud computing assistance International Symposium on VLSI Design, Automation and Test (VLSI-DAT), Apr. 2018.

指導教授　楊家驥 教授

現職
- Professor, Department of Electrical Engineering and Graduate Institute of Electronics Engineering, National Taiwan University

學歷
- Ph.D. (2010) in Electrical Engineering, University of California at Los Angeles
- M.S. (2004) and B.S. (2002) in Electrical Engineering, National Taiwan University

經歷
- TPC Member, International Solid-State Circuits Conference (ISSCC)
- TPC Member, Symposium on VLSI Circuits (VLSI Circuits)
- TPC Member, Asian Solid-State Circuit Conference (A-SSCC)
- Senior Associate Editor, IEEE Signal Processing Letters (SPL)
- Guest Editor, IEEE Journal of Solid-State Circuits (JSSC)

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獲獎摘要

王宇瑄同學自 2019 年起於國立陽明交通大學電子研究所攻讀博士班，博士班期間專注於低溫多晶矽薄膜電晶體 (Low-Temperature Polycrystalline Silicon Thin-Film Transistors) 與第三代半導體元件可靠度物理機制探討及可撓式顯示器的結構設計開發。於釐清元件的性能 / 可靠度劣化議題後，提出相對應的結構設計 / 製程改善方案，所提出的新穎結構在 2019 年發表於 IEEE IEDM。迄今，其研究成果以第一作者共發表 4 篇 SCI 國際期刊於 IEEE EDL / IEEE TED 等國際期刊。王同學於 2021 年獲「科技部補助博士生赴國外研究」，將以訪問學者身分前往加拿大英屬哥倫比亞大學進行研究。

得獎經歷

- 2022 陳龍英教授獎學金
- 2021 科技部補助博士生赴國外研究
- 2020 台積電博士班獎學金
- 2019 鑫淼重點科技博士班獎學金
- 2019 國立交通大學卓越博士獎學金
- 2019 平安菁英教育基金會菁英獎學金
- 2018 教育部台灣能潔能科技創意實作競賽佳作

重要學術著作

1. **Y.-X. Wang,** S.-P. Huang, M.-C. Tai, et. al, "A Novel Structure Serving as a Stress Relief Layer for Flexible LTPS TFTs", 2019 IEEE International Electron Device Meetings (IEEE IEDM), San Francisco, CA, USA
2. **Y.-X. Wang,** T.-C. Chang, M.-C. Tai, et. al, "Investigation of Degradation Behavior during Illuminated Negative Bias Temperature Stress in P-channel Low Temperature Polycrystalline Silicon Thin-Film Transistors," IEEE Electron Device Letters, vol. 42, no. 5, pp. 712-715, Mar. 2021.
3. **Y.-X. Wang,** T.-C. Chang, S.-P. Huang, et. al, "A Novel Structure to Reduce Degradation Under Mechanical Bending in Foldable Low Temperature Polysilicon TFTs Fabricated on Polyimide," IEEE Electron Device Letters, vol. 41, no. 5, pp. 725-728, May. 2020.
4. **Y.-X. Wang,** T.-C. Chang, M.-C. Tai, et. al, "Improvement of Strained Negative Bias Temperature Instability in Flexible LTPS TFTs by a Stress-Release Design," IEEE Transactions on Electron Devices, vol. 69, no. 3, pp. 1532-1537, Jan. 2022.
5. **Y.-X. Wang,** M.-C. Tai, T.-C. Chang, et. al, "Suppression of Edge Effect Induced by Positive Gate Bias Stress in Low Temperature Polycrystalline Silicon TFTs with Channel Width Extension over Source/Drain Regions," IEEE Transactions on Electron Devices, vol. 67, no. 12, pp. 5552-5556, Nov. 2020.
6. A. Sood, F.-G. Tarntair, **Y.-X. Wang,** et. al, "Performance enhancement of ZnGa2O4 Schottky type deep-ultraviolet photodetectors by oxygen supercritical fluid treatment," Results in Physics, vol. 29, pp. 104764, Oct. 2021.
7. M.-C. Tai, **Y.-X. Wang,** T.-C. Chang, et. al, "Gate Dielectric Breakdown in a-InGaZnO Thin Film Transistors with Cu Electrodes" IEEE Electron Device Letters, vol. 42, no. 6, pp. 851-854, Apr. 2021.
8. M.-C. Tai, **Y.-X. Wang,** T.-C. Chang, et. al, "Heterojunction Channels in Oxide Semiconductors for Visible-Blind Nonvolatile Optoelectronic Memories," Advanced Electronic Materials, vol. 6, no. 11, pp. 2000747, Oct. 2020.
9. C.-C. Lin, M.-C. Tai, T.-C. Chang, Y.-C. Tsao, **Y.-X. Wang,** et. al, "Interface Defect Shielding of Electron Trapping in a-InGaZnO Thin Film Transistors," IEEE Transactions on Electron Devices, vol. 67, no. 9, pp. 3645-3649, Aug. 2020.
10. **Y.-X. Wang,** C.-I. Yang, Y.-Z. Zheng, et. al, "The Effect of R=1mm Mechanical Bending Strain on Wing-Shape Structural Foldable Low Temperature Polysilicon TFTs Fabricated on Polyimide," Symposium on Nano Device Technology, Hsinchu, Taiwan, 2018. (Best Student Paper Award)

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經歷　・ IEEE Fellow
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獲獎摘要

吳明鴻同學自 2017 年起於國立陽明交通大學電子研究所 - 固態組攻讀博士班。主要研究領域為磁阻式記憶體於脈衝類神經網路加速器應用設計及低能耗高可靠度鐵電式記憶體開發。其研究成果於 VLSI、IEDM、DAC 等 IEEE 頂尖國際會議發表。

得獎經歷 / 專利

- 2021 陳龍英教授獎學金
- 2020 台積電獎學金
- 以第五發明人發表美國專利，Patent number：USP 16,809,522

重要學術著作

1. **M.-H. Wu,** M.-C. Hong, C.-C. Chang, P. Sahu, J.-H. Wei, H.-Y. Lee, S.-S. Sheu, and T.-H. Hou, "Extremely Compact Integrate-and-Fire STT-MRAM Neuron: A Pathway toward All-Spin Artificial Deep Neural Network," 2019 Symposium on VLSI Technology, 2019, pp. T34-T35.
2. **M.-H. Wu,** M.-S. Huang, Z. Zhu, F.-X. Liang, M.-C. Hong, J. Deng, J.-H. Wei, S.-S. Sheu, C.-I Wu, G. Liang and T.-H. Hou, "Compact Probabilistic Poisson Neuron Based on Back-Hopping Oscillation in STT-MRAM for All-Spin Deep Spiking Neural Network," 2020 IEEE Symposium on VLSI Technology, 2020, pp. 1-2.
3. M.-H. Yan, **M.-H. Wu,** H.-H. Huang, Y.-H. Chen, Y.-H. Chu, T.-L. Wu, P.-C. Yeh, C.-Y. Wang, Y.-D. Lin, J.-W. Su, P.-J. Tzeng, S.-S. Sheu, W.-C. Lo, C.-I Wu, and T.-H. Hou, "BEOL-Compatible Multiple Metal-Ferroelectric-Metal (m-MFM) FETs Designed for Low Voltage (2.5 V), High Density, and Excellent Reliability," 2020 IEEE International Electron Devices Meeting (IEDM), 2020, pp. 4.6.1-4.6.4.
4. C.-C. Chang, **M.-H. Wu,** J.-W. Lin, C.-H. Li, V. Parmar, H.-Y. Lee, J.-H. Wei, S.-S. Sheu, M. Suri, T.-S. Chang, and T.-H. Hou, "NV-BNN: An Accurate Deep Convolutional Neural Network Based on Binary STT-MRAM for Adaptive AI Edge," 2019 56th ACM/IEEE Design Automation Conference (DAC), 2019, pp. 1-6.
5. T.-Y. Wu, H.-H. Huang, Y.-H. Chu, C.-C. Chang, **M.-H. Wu,** C.-H. Hsu, C.-T. Wu, M.-C. Wu, W.-W. Wu, T.-S. Chang, H.-Y. Lee, S.-S. Sheu, W.-C. Lo, and T.-H. Hou, "Sub-nA Low-Current HZO Ferroelectric Tunnel Junction for High-Performance and Accurate Deep Learning Acceleration," 2019 IEEE International Electron Devices Meeting (IEDM), 2019, pp. 6.3.1-6.3.4.
6. H.-H. Huang, T.-Y. Wu, Y.-H. Chu, **M. -H. Wu,** C.-H. Hsu, H.-Y. Lee, S.-S. Sheu, W.-C. Lo, and T.-H. Hou, "A Comprehensive Modeling Framework for Ferroelectric Tunnel Junctions," 2019 IEEE International Electron Devices Meeting (IEDM), 2019, pp. 32.2.1-32.2.4.
7. C.-C. Chang, J.-C. Liu, Y.-L. Shen, T. Chou, P.-C. Chen, I-T. Wang, C.-C. Su, **M.-H. Wu,** B. Hudec, C.-C. Chang, C.-M. Tsai, T.-S. Chang, H.-P. Wong, T.-H. Hou, "Challenges and opportunities toward online training acceleration using RRAM-based hardware neural network," 2017 IEEE International Electron Devices Meeting (IEDM), 2017, pp. 11.6.1-11.6.4.

指導教授　侯拓宏 特聘教授

現職　・國立陽明交通大學
學歷　・康乃爾大學 / 電機工程博士 (2004~2008)
經歷　・國立陽明交通大學 / 電子研究所特聘教授 (2021~ 迄今)

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獲獎摘要

林智斌同學於 2016 年在國立陽明交通大學電子研究所攻讀博士班。研究領域專注在二維材料合成及奈米電子元件製程與應用。林同學的研究成果包含以第一作者發表的 3 篇國際期刊論文與 4 篇國際會議論文；另外，也與友達光電股份有限公司進行產學合作，並擁有一個中華民國專利。

得獎經歷

- 2020 交通大學電機院學生榮獲重要學術獎
- 中華民國專利「電子裝置與其製造方法」第七發明人
- 2016 交大台積電聯合研發中心獎助學金

重要學術著作

1. **C.-P. Lin,** H.-H Hsu, J.-H. Huang, Y.-W. Kang, C.-T. Wu, Y. –J. Lee, C.-C. Cheng, Y.-W. Lan, W.-H. Chang, L.-J. Li, and T.-H. Hou*, "Two-dimensional solid-phase crystallization toward centimeter-scale monocrystalline layered $MoTe_2$ via two-step annealing," J. Mater. Chem. C, vol. 9, pp. 15566-15576, 2021.
2. **C.-P. Lin,** P.-C. Chen, J.-H. Huang, C.-T. Lin, D. Wang, W.-T. Lin, C.-C. Cheng, C.-J. Su, Y.-W. Lan, and T.-H. Hou*, "Local modulation of electrical transport in 2D layered Materials induced by electron beam irradiation," ACS Appl. Electron. Mater., vol. 1, pp. 684-691, 2019.
3. (co-first author) P.-C. Chen, **C.-P. Lin,** C.-J. Hong, C.-H. Yang, Y.-Y. Lin, M.-Y. Li, L.-J. Li, T.-Y. Yu, C. –J. Su, K.-S. Li, Y.-L. Zhong, T.-H. Hou*, and Y.-W. Lan, "Effective N-methyl-2-pyrrolidone wet cleaning for fabricating high-performance monolayer MoS_2 transistors," Nano Res., vol. 12, pp. 303-308, 2019.
4. (invited) **C.-P. Lin,** Y.-W. Kang, C.-P. Hsu, H.-H. Hsu, J.-H. Huang, R.-F. Chen, C.-T. Wu, Y.-J. Lee, and T.-H. Hou*, "Monolithic 3D integration of 2D electronics based on two-dimensional solid-phase crystallization," 2021 Symposium on VLSI Technology, Kyoto, Japan, 2021, pp. 1-2.
5. **C.-P. Lin,** H.-H. Hsu, and T.-H. Hou*, "Phase and carrier polarity control of sputtered $MoTe_2$ by plasma-induced defect engineering," 2020 Device Research Conference (DRC), Columbus, OH, USA, 2020, pp. 1-2.
6. (invited) **C.-P. Lin,** C.-T. Lin, P.-S. Liu, M.-J. Yu, and T.-H. Hou*, "Grain size and plasma doping effects on CVD-based 2D transition metal dichalcogenide," 2016 IEEE 16th International Conference on Nanotechnology (IEEE-NANO), Sendai, Japan, 2016, pp. 501-504.
7. **C.-P. Lin,** L.-S. Lyu, C.-T. Lin, P.-S. Liu, W.-H. Chang, L.-J. Li, and T.-H. Hou*, "Grain size effect of monolayer MoS_2 transistors characterized by second harmonic generation mapping," 2015 IEEE 22nd International Symposium on the Physical and Failure Analysis of Integrated Circuits, Hsinchu, Taiwan, 2015, pp. 476-479.
8. C.-J. Liu, Y. Wan, L.-J. Li, **C.-P. Lin,** T.-H. Hou*, Z.-Y. Huang, and V. P.-H. Hu, "2D materials-based static random-access memory," Adv. Mater., p. 2107894, 2022.
9. K.-W. Chen, S.-J. Chang, E. Y.-T. Tang, **C.-P. Lin,** T.-H. Hou*, C.-H. Chen, and Y.-C. Tseng, "Pulse-mediated electronic tuning of the MoS_2-perovskite ferroelectric field effect transistors," ACS Appl. Electron. Mater., vol. 2, pp. 3843-3852, 2020.

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・科技部 A 世代半導體專案計畫召集人
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獲獎摘要

邱硯晟同學自 2019 年起於國立清華大學電機工程學系 - 系統組攻讀博士班。主要研究領域為應用於人工智能晶片之記憶體內運算 (Computing-In-Memory) 電路設計和記憶體安全相關之電路設計。其中包含了揮發性記憶體內運算設計 (SRAM-CIM)、非揮發性記憶體內運算設計 (PCRAM-CIM, MRAM-CIM) 以及非揮發性記憶體安全保護電路。其研究成果於國際頂級期刊 Nature Electronics, JSSC 及 ISSCC, IEDM, ASSCC 等 IEEE 頂尖國際會議發表。

得獎經歷

- 2021 台積電研究助理獎學金
- 2020 台積電研究助理獎學金
- 2020 旺宏金矽獎銅獎
- 2019 科技部 - 培育優秀博士生獎學金
- 2019 台積電研究助理獎學金
- 2018 台積電研究助理獎學金

重要學術著作

1. **Y.-C. Chiu** et al., " A 22nm 4Mb STT-MRAM data-encrypted Near-Memory-Computation Macro with 192GB/s Read-and-Decryption Bandwidth and 25.1-55.1 TOPS/W at 8b MAC for AI-oriented Operations" IEEE International Solid-State Circuit Conference (ISSCC) 2022
2. W-S. Khwa*, **Y-C. Chiu*** et al., "A 40-nm, 2M-Cell, 8b-Precision, Hybrid SLC-MLC PCM Computing-in-Memory Macro with 20.5 - 65.0TOPS/W for Tiny-AI Edge Devices," 2022 IEEE International Solid- State Circuits Conference (ISSCC), 2022, pp. 1-3 (*Equally-Credicted Authors, ECAs)
3. **Y.-C. Chiu** et al., "A 22-nm 1-Mb 1024-b Read Data-Protected STT-MRAM Macro With Near-Memory Shift-and-Rotate Functionality and 42.6-GB/s Read Bandwidth for Security-Aware Mobile Device," in IEEE Journal of Solid-State Circuits
4. Xue, CX*., **Chiu, YC***., Liu, TW. et al. A CMOS-integrated compute-in-memory macro based on resistive random-access memory for AI edge devices. Nat Electron 4, 81–90 (2021) (Xue, CX*., Chiu, YC* contribute equally)
5. **Y.-C. Chiu** et al., "A 4-Kb 1-to-8-bit Configurable 6T SRAM-Based Computation-in-Memory Unit-Macro for CNN-Based AI Edge Processors," in IEEE Journal of Solid-State Circuits, vol. 55, no. 10, pp. 2790-2801, Oct. 2020
6. **Y.-C. Chiu** et al., "A 40nm 2Mb ReRAM Macro with 85% Reduction in FORMING Time and 99% Reduction in Page-Write Time Using Auto-FORMING and Auto-Write Schemes," 2019 Symposium on VLSI Technology, 2019, pp. T232-T233
7. T.-C. Chang, ⋯ **Yen-Cheng Chiu** et al., "13.4 A 22nm 1Mb 1024b-Read and Near-Memory-Computing Dual-Mode STT-MRAM Macro with 42.6GB/s Read Bandwidth for Security-Aware Mobile Devices," 2020 IEEE International Solid- State Circuits Conference - (ISSCC), 2020, pp. 224-226
8. X. Si ⋯ **Yen-Cheng Chiu** et al., "24.5 A Twin-8T SRAM Computation-In-Memory Macro for Multiple-Bit CNN-Based Machine Learning," 2019 IEEE International Solid- State Circuits Conference - (ISSCC), 2019, pp. 396-398

指導教授　張孟凡 教授

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・台灣積體電路製造公司 (TSMC) Director of Corporate Research (2020~)
・ IEEE Taipei Section Chair (2019/1-2021/1)
・科技部 Program Director, Micro-Electronics Program (2018/1-2020/12)
・國立清華大學 / 電機工程學系特聘教授 (2019/8 ~)
・國立清華大學 / 電機工程學系教授 (2014/8)
・國立清華大學 / 電機工程學系副教授 (2006/8)

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獲獎摘要

王家慶同學於 2016 年進入國立成功大學電機工程學系博士班，就讀期間研究混合訊號與高解析高速資料轉換器 IC 設計，包含多項高解析低功耗導管逐漸趨近式 (Pipelined-SAR) 及高速次區間式 (Subranging) 類比數位轉換器 (ADC) 設計技術。該生嫻熟於先進製程類比電路設計，博士班期間已完成至少 5 次晶片下線，並成功量測驗證預期規格，效能卓越。研究成果已發表於 2020、2022 年之 IEEE International Solid-State Circuits Conference (ISSCC) 以及 2020 年 IEEE Journal of Solid-State Circuits (JSSC) 等 IC 設計領域之旗艦級國際研討會與期刊，並受 IC 設計公司青睞，實現技術移轉，其中多項重點技術規格均於發表當時刷新世界紀錄。除了現有卓越研究貢獻，該生尚有多項傑出成果等待發表。

得獎經歷

- 2021 聯詠科技 (Novatek) 博士班獎學金
- 2020 國研院台灣半導體研究中心 (TSRI) 特別設計獎
- 2016 中華民國斐陶斐榮譽學會榮譽會員
- 2016 中國工程師學會 (CIE) 優秀工程學生獎學金
- 2016 成大電機系大學部全系第一名畢業

重要學術著作

1. **Jia-Ching Wang** (Presenting author), Bing-Yang Li, and Tai-Haur Kuo, "A 9.8-fJ/conv.-step FoMw 8b 2.5-GS/s Single-Channel CDAC-Assisted Subranging ADC with Reference-Embedded Comparators," accepted by and to be presented in IEEE Symposium on VLSI Circuits (VLSIC), June 2022.
2. **Jia-Ching Wang** (Presenting author) and Tai-Haur Kuo, "A 0.82-mW 14-bit 130-MS/s Pipelined-SAR ADC with a Distributed Averaging Correlated Level Shifting (DACLS) Ringamp and Bypass-Window Backend," in IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers, pp. 162-163, Feb. 2022.
3. **Jia-Ching Wang,** Tsung-Chih Hung, and Tai-Haur Kuo*, "A Calibration-Free 14-b 0.7-mW 100-MS/s Pipelined-SAR ADC Using a Weighted-Averaging Correlated Level Shifting Technique, "IEEE J. Solid-State Circuits, vol. 55, no. 12, pp. 3271-3280, Dec. 2020.
4. Tsung-Chih Hung, **Jia-Ching Wang** (Presenting author), and Tai-Haur Kuo, "A Calibration-Free 71.7dB SNDR 100MS/s 0.7mW Weighted-Averaging Correlated Level Shifting Pipelined SAR ADC with Speed-Enhancement Scheme," in IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers, pp. 256-257, Feb. 2020.

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獲獎摘要

胡愷育同學自 2017 年起就讀國立成功大學電機工程學系博士班，目前主要研究領域為數位控制電源管理晶片設計，博士班研究成果共發表三篇第一作者 IEEE 期刊論文，四篇第一作者 IEEE 會議論文，六項專利，包含兩項美國專利、兩項中國專利及兩項中華民國專利。

得獎經歷 / 專利

- 「第十八屆旺宏金矽獎 設計組」優勝獎
- 「教育部 107 學年度大學校院積體電路設計競賽，類比電路設計組」特優
- 「教育部 106 學年度大學校院積體電路設計競賽，類比電路設計組」佳作
- 「 2016 CIC 晶片製作，類比組」特優設計
- 獲得六項專利，包含兩項美國專利、兩項中國專利及兩項中華民國專利

重要學術著作

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8. Yi-Hua Chang, **Kai-Yu Hu,** Guan-Shen Yao, Chun-Yu Chen and Chien-Hung Tsai, "Mixed-Level Design Methodology for Digitally Controlled Power Converter IC," 2018 IEEE 7th Global Conference on Consumer Electronics (GCCE), Nara, Japan, 2018, pp. 811-812
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10. Jing-Teng Lin, **Kai-Yu Hu** and Chien-Hung Tsai, "Digital multiphase buck converter with current balance/phase shedding control," TENCON 2015 - 2015 IEEE Region 10 Conference, Macao, China, 2015

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獲獎摘要

陳建傑同學自 2018 年起於國立中山大學物理所攻讀博士班。主要研究領域為薄膜電晶體 (Thin Film Transistor)，其主動層材料包含低溫多晶矽（Low-temperature polycrystalline silicon，LTPS）、非晶銦鎵鋅氧（Amorphous. InGaZnO, a-IGZO）與有機材料（Organic）。深入探討其大電流操作下的熱載子效應 (Hot-carrier Effect) 與自熱效應 (Self-heating Effect)、因製程中乾式蝕刻 (Dry Etching) 造成的異常漏電等相關物理機制，並提出相應解決方案。研究成果共發表 4 篇國際期刊，分別發表 EDL 3 篇、TED 1 篇之 IEEE 頂尖國際期刊。

得獎經歷

- 2022 友達光電人才培育獎學金
- 2021 年獲得友達光電第十八屆 A+ 暑期實習 - 優等
- 110 年度 國防工業獎學金

重要學術著作

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7. Y.-H. Hung, T.-C. Chang, ⋯**J.-J. Chen,** et.al, “Investigation of Thermal Behavior on High-Performance Organic TFTs Using Phase Separated Organic Semiconductors,” IEEE Electron Device Letters, vol. 42, no. 6, pp. 859–862, 2021.
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